REMARKS/ARGUMENTS

The Examiner is thanked for the Office Action dated September 18, 2007. The status of the application is as follows:

- Claims 21 and 24-40 are pending. Claim 21 has been amended to include aspects of claim 22. Claim 22 has been cancelled. Claims 25, 31, 37 and 38 have also been amended.
- Claims 21 and 24-40 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of co-pending Application No. 10/730,319.
- Claims 31, 32, 35, 36 and 38 are rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. (US Pub 2002/0169922) in view of Pollard, II et al. (US 7,050,959).
- Claims 21, 24-27, 29, 34 and 40 are rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. in view of Pollard, II et al. and further in view of Huang (US Pub 2003/0095464).
- Claims 28, 33 and 39 are rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. in view of Pollard, II and further in view of Mylly (US Pub. 2005/0235110).
- Claims 30 and 37 are rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. and Pollard, II and further in view of Jeddeloh (US Pub. 2002/0144173).
- These rejections are discussed below.

The Provisional Rejection

Claims 21 and 24-40 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of co-pending Application No. 10/730,319. This rejection will be addressed at a later time in the event that Application No. 10/730,319 issues as a patent.

The Rejection of Claims 31, 32, 35, 36 and 38 Under 35 U.S.C. §103(a)

Claims 31, 32, 35, 36 and 38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. in view of Pollard, II et al. This rejection should be withdrawn because the combination of Thomann et al. and Pollard, II et al. does not to teach or suggest all the claim limitations and, thus, fails to establish a *prima facie* case of obviousness.

> To establish a *prima facie* case of obviousness... the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP §2142

Independent **claim 31** has been amended to include aspects of claim 37, which depends from claim 31. As such, the amendment to claim 31 does not necessitate any further search. Amended claim 31 recites, *inter alia,* that the acquired first memory attribute information and the acquired second memory attribute information include Serial Presence Detect information. The Office concedes that the combination of Thomann et al. and Pollard, II et al. does not teach or suggest these claim aspects. Accordingly, this rejection should be withdrawn.

Claim 35, which depends from claim 31, recites accessing a setting value candidate database, using at least a portion of the first memory attribute information as an index with respect to contents of the setting value candidate database to determine the first data transfer rate setting value, and using at least a portion of the second memory attribute information as an index with respect to contents of the setting value candidate database to determine the second data transfer rate setting value. For this rejection, the Office states that the rejection of claim 38 applies. However, the sections of the references cited in the rejection of claim 38 are devoid of any teaching or suggestion regarding using at least a portion of memory attribute information as an index with respect to contents of the setting value candidate database to determine the data transfer rate setting value. Therefore, this rejection should be withdrawn.

Claim 36, which depends from claim 31, recites, *inter alia,* determining the first data transfer rate setting value based at least in part upon the first upper limit temperature, and determining the second data transfer rate setting value based at least in part upon the second upper limit temperature. The Office references Pollard, II et al. column 3, lines 30-48, to teach these claim aspects. In contrast, this section of Pollard, II et al. discloses that the ROM 145 stores memory module design characteristics including a maximum allowable junction temperature and that the BIOS 110 utilizes a combination of thermal environment characteristics and memory module design characteristics to determine a maximum sustainable power level for an integrated circuit, where the "maximum sustainable power level" is defined as an amount of operational power that an integrated circuit can dissipate given a particular thermal environment so as to not exceed specified minimum and/or maximum temperature thresholds. Hence, the ROM stores design characteristics such a maximum allowable junction temperature and the BIOS 110 utilizes

thermal environment and memory module design characteristics to determine a maximum sustainable power level. However, column 3, lines 30-48, is devoid of any teaching or suggestion regarding an upper limit temperature, let alone determining a data transfer rate setting value based at least in part upon an upper limit temperature. In view of the foregoing, withdrawal of this rejection is respectfully requested.

Independent **claim 38** has been amended to recite that the computer-readable medium comprises computer-executable instructions for, *inter alia*, locating candidate data transfer rate setting values for each memory module in the plurality of memory modules in the setting value candidate database, wherein the candidate data transfer rate setting values correspond to the acquired memory attribute information in the setting value candidate database, obtaining current data transfer rates for the each of the memory modules in the plurality of memory modules, wherein the current data transfer rate is the data transfer rate currently being used to transfer data, comparing the current and the candidate data transfer rates, and determining a data transfer rate setting value that is to be applied with respect to each memory module in the plurality of memory modules based at least in part upon the comparison. The combination of Thomann et al. and Pollard, II et al. does not teach or suggest these claim aspects. Therefore, this rejection should be withdrawn.

Claim 32 depends from claim 31 and is allowable at least by virtue of this dependency.

The Rejection of Claims 21, 24-27, 29, 34 and 40 Under 35 U.S.C. §103(a)

Claims 21, 24-27, 29, 34 and 40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. in view of Pollard, II et al. and further in view of Huang. This rejection should be withdrawn because the combination of Thomann et al., Pollard, II et al. and Huang does not to teach or suggest all the claim limitations and, thus, fails to establish a *prima facie* case of obviousness.

Independent **claim 21** has been amended to include aspects of claim 22. As such, the amendment to claim 21 does not necessitate any further search. Amended claim 21 now also recites, *inter alia*, receiving an upper limit temperature at which each memory module in the multiple memory modules is operated, and individually determining data transfer rates for each memory module in the multiple memory modules based at least in part upon all of the corresponding received memory module attribute information, the received upper limit temperature, and the received attachment position information.

The Office references Thomann et al., paragraph [0055], and Pollard, II et al. column 3, lines 30-39, to teach receiving an upper limit temperature at which each memory module in the multiple memory modules is operated. The Office references Thomann et al., paragraph [0063], to teach individually determining data transfer rates for each memory module in the multiple memory modules based at least in part upon all of the corresponding received memory module attribute information, the received upper limit temperature, and the received attachment position information. However, the referenced sections of Thomann et al. and Pollard, II et al. do not teach or suggest the subject claim limitations.

More particularly, Thomann et al., at paragraph [0055], discloses that environmental conditions such as temperature and humidity can affect the speed at which a memory device can transmit data. However, this refers to the environmental conditions in which the memory device is operating in, whereas claim 21 requires the temperature be that at which the memory module is operated. The temperature of the environment does not teach or suggest an upper limit temperature at which each memory module in the multiple memory modules is operated.

Pollard, II et al., at column 3, lines 30-39, discloses that a ROM 145 stores memory module design characteristics including the number of devices on the module, active, idle, and standby power consumption levels of each device on the module, substrate height, heat spreader design data, a maximum allowable junction temperature, and so forth. However, design characteristics such as a maximum allowable junction temperature stored in a ROM do not teach or suggest an upper limit temperature at which each memory module in the multiple memory modules is operated.

Thomann et al., at paragraph [0063], discloses that for DQ level calibration, read/write timing calibration is performed individually for all DQ lines 143 on all memory modules within a computer system. Thus, this section of Thomann et al. is devoid of any teaching or suggestion regarding individually determining data transfer rates for each memory module in the multiple memory modules based at least in part upon all of the corresponding received memory module attribute information, the received upper limit temperature, and the received attachment position information.

In view of the above, it is readily apparent that Thomann et al. and Pollard, II et al. individually and in combination, do not teach or suggest all the limitations of claim 21. As such, the rejection of claim 21 should be withdrawn.

Amended **claim 25**, which depends from claim 21, recites retrieving a candidate data transfer rate from the setting value candidate database for at least one memory module in the multiple memory modules, the candidate data transfer rate from the setting value candidate database is located based at least in part upon memory attribute information stored in the at least one memory module, determining a current data transferring rate, which is the data transfer rate currently being used to transfer data, comparing the current and the candidate data transfer rates, and setting the data transfer rate based on the comparison. The combination of Thomann et al., Pollard, II et al. and Huang does not teach or suggest such claim aspects. Therefore, this rejection should be withdrawn.

Claim 27, which depends from claim 21, recites, *inter alia,* determining a maximum data transfer rate with respect to data transfer rates determined for each memory module, determining a minimum data transfer rate with respect to data transfer rates determined for each memory module, and collectively setting the data transfer rate with respect to the multiple memory modules as a value that is between the maximum data transfer rate and the minimum data transfer rate. The Office references Pollard, II et al. column 3, lines 40-52, column 4, lines 46-57, and column 5, lines 4-9, to teach these aspects.

However, column 3, lines 40-52, discloses that a BIOS 110 utilizes a combination of thermal environment characteristics and memory module design characteristics to determine a maximum sustainable power level for an integrated circuit, where "maximum sustainable power level" is defined as an amount of operational power that an integrated circuit can dissipate given a particular thermal environment so as to not exceed specified minimum and/or maximum temperature thresholds. Column 3, lines 40-52, does not teach or suggest determining a minimum data transfer rate.

Column 5, lines 4-9, discloses that once the maximum performance characteristic (e.g. bandwidth) of the integrated circuit is determined, the system adjusts operation of the integrated circuit so as to keep operating temperatures within a specified range. In one embodiment, BIOS 110 adjusts operation of memory module 140 to maintain operating temperatures within a specified range, whereas in an alternative embodiment, chipset 120 may adjust the operation of memory module 140 to maintain such a temperature range. Hence, this section of Pollard teaches operating an integrated circuit based on temperatures, and not minimum and maximum data transfer rates.

Thus, Pollard, II et al. does not teach or suggest determining a minimum data transfer rate with respect to data transfer rates determined for each memory module or collectively setting the data transfer rate with respect to the multiple memory modules as a value that is between the maximum data transfer rate and the minimum data transfer rate. Therefore, this rejection should be withdrawn.

Claims 24, 26, 29, 34 and 40 directly or indirectly depend from independent claims 21, 31 and 38 and are allowable at least by virtue of their dependencies.

The Rejection of Claims 28, 33 and 39 Under 35 U.S.C. §103(a)

Claims 28, 33 and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. in view of Pollard, II et al. and further in view of Mylly. **Claims 28, 33 and 39** depend from independent claims 21, 31 and 38 and are allowable at least by virtue of their dependencies.

The Rejection of Claims 30 and 37 Under 35 U.S.C. §103(a)

Claims 30 and 37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann et al. in view of Pollard, II et al. and further in view of Jeddeloh. This rejection should be withdrawn because the combination of Thomann et al., Pollard, II et al. and Jeddeloh does not to teach or suggest all the claim limitations and, thus, fails to establish a *prima facie* case of obviousness.

Claim 37, which depends from claim 31, has been amended to recite, *inter alia,* determining the data transfer rate setting value according to a heating value, which is determined in accordance with a total number of memory devices implemented in the memory module, an implementation state of the memory devices, a type of the memory devices, and a manufacturer of the memory devices. The combination of Thomann et al., Pollard, II et al. and Jeddeloh does not teach or suggest these claimed aspects. Accordingly, this rejection should be withdrawn.

Claim 30 depends from independent claim 21 and is allowable at least by virtue of this dependency.

Conclusion

It is believed that each of the claims now in the application is distinguishable one from the other and over the prior art. Therefore, reconsideration and allowance of the claims is respectfully requested.

Respectfully submitted,

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By: _____
Anthony M. Del Zoppo, Reg. No. 51,606
CUSTOMER NO. 56687

AMD:cg